Abstract

Memory Cell Array Comprising Individually Addressable Memory Cells and Method of Making the Same

A memory cell array comprises a plurality of memory transistors arranged in a two-dimensional array, each memory transistor having two source/drain regions arranged in a first direction of the memory cell array with a channel substrate region therebetween, and a gate structure arranged above the channel substrate region. The source/drain regions and channel substrate regions are formed in a substrate arranged on an insulating layer, with the channel substrate regions of memory transistors adjacent each other in the first direction being separated from each other by respective source/drain regions extending down to the insulating layer. The source/drain regions and the channel substrate regions of memory transistors adjacent each other in a second direction of the memory cell array furthermore are isolated from each other by trenches filled with insulating material and formed in the substrate so as to extend down to the insulating layer.